Digital-To-Analog Converters

Introduction

Digital-to-analog converters are the devices by which computers communicate with the outside world. They are employed in a variety of applications from CRT display systems and voice synthesizers to automatic test systems, digitally controlled attenuators, and process control actuators. In addition, they are key components inside most A/D converters. D/A converters are also referred to as DAC’s and are termed decoders by communications engineers.

The transfer function of an ideal 3-bit D/A converter is shown in Figure 1. Each input code word produces a single, discrete analog output value, generally a voltage. Over the output range of the converter, different values are produced including zero; and the output has a one-to-one correspondence with input, which is not true for A/D converters.

There are many different circuit techniques used to implement D/A converters, but a few popular ones are widely used today. Virtually all D/A converters in use are of the parallel type where all bits change simultaneously upon application of an input code word; serial type D/A converters, on the other hand, produce an analog output only after receiving all digital input data in sequential form.

Weighted Current Source D/A Converter

The most popular D/A converter design in use today is the weighted current source circuit illustrated in Figure 2. An array of switched transistor current sources is used with binary weighted currents. The binary weighting is achieved by using emitter resistors with binary related values of R, 2R, 4R, 8R, ..., 2^N. The resulting collector currents are then added together at the current summing line.

The current sources are switched on or off from standard TTL inputs by means of the control diodes connected to each emitter. When the TTL input is high, the current source is on; when the input is low it is off, with the current flowing through the control diode. Fast switching speed is achieved because there is direct control of the transistor current, and the current sources never go into saturation.

To interface with standard TTL levels, the current sources are biased to a base voltage of ±1.2V. The emitter currents are regulated to constant values by means of the control amplifier and a precision voltage reference circuit together with a bipolar transistor.

The sum of output currents from all current sources that are on goes to an operational amplifier summing junction; the amplifier converts this output current into an output voltage. In some D/A converters the output current is used to directly drive a resistor load for maximum speed, but the positive output voltage in this case is limited to about ±1 volt.

The weighted current source design has the advantages of simplicity and high speed. Both PNP and NPN transistor current sources can be used with this technique although the TTL interfacing is more difficult with NPN sources. This technique is used in most monolithic, hybrid, and modular D/A converters in use today.

A difficulty in implementing higher resolution D/A converter designs is that a wide range of emitter resistors is required, and very high value resistors cause problems with both temperature stability and switching speed. To overcome these problems, weighted current sources are used in identical groups, with the output of each group divided down by a resistor divider as shown in Figure 3.

The resistor network B, divided by B1 and B2, divides the output of Group 3 down by a factor of 256 and the output of Group 2 down by a factor of 16 with respect to the output of Group 1. Each group is identical, with four current sources of the type shown in Figures 2, having binary current weights of 1, 2, 4, and 8. The output of Figure 3 also illustrates the method of achieving a bipolar output by deriving an offset current from the reference circuit which is then subtracted from the output current line through resistor R4. The current is set to exactly one half the full scale output current.
R-2R D/A Converter
A second popular technique for D/A conversion is the R-2R ladder method. As shown in Figure 4, the network consists of series resistors of value R and shunt resistors of value 2R. The bottom of each shunt resistor has a single-pole double-throw electronic switch which connects the resistor to either ground or the output current summing line.

The operation of the R-2R ladder network is based on the binary division of current as it flows down the ladder. Examination of the ladder configuration reveals that at point A looking to the right, one measures a resistance of 2R; therefore the reference input to the ladder has a resistance of R. At the reference input the current splits into two equal parts since it sees equal resistances in either direction. Likewise, the current flowing down the ladder to the right continues to divide into two equal parts at each resistor junction.

The result is binary weighted currents flowing down each shunt resistor in the ladder. The digitally controlled switches direct the currents to either the summing line or ground. Assuming all bits are on as shown in the diagram, the output current is

\[ I_{out} = \frac{V_{ref}}{R} \left( \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \ldots + \frac{1}{2^n} \right) \]

which is a binary series. The sum of all currents is then

\[ I_{out} = \frac{V_{ref}}{R} \left( 1 - 2^{-n} \right) \]

where the \(2^{-n}\) term physically represents the portion of the input current flowing through the 2R terminating resistor to ground at the far right.

As in the previous circuit, the output current summing line goes to an operational amplifier which converts current to voltage.

The advantage of the R-2R ladder technique is that only two values of resistors are required, with the resultant ease of matching or trimming and excellent temperature tracking. In addition, for high speed applications relatively low resistor values can be used. Excellent results can be obtained for high resolution D/A converters by using laser-trimmed thin-film resistor networks.

Multiplying and Deglitched D/A Converters
The R-2R ladder method is specifically used for multiplying type D/A converters. With these converters, the reference voltage can be varied over the full range of \( \pm V_{max} \) with the output the product of the reference voltage and the digit input word. Multiplication can be performed in 1, 2, or 4 algebraic quadrants.

If the reference voltage is unipolar, the circuit is a one-quadrant multiplying DAC. If it is bipolar, the circuit is a two-quadrant multiplying DAC. For four-quadrant operation the two current summing lines shown in Figure 4 must be subtracted from each other by operational amplifiers.

In multiplying D/A converters, the electronic switches are usually implemented with CMOS devices. Multiplying DAC's are commonly used in automatic gain controls, CRT character generation, complex function generators, digital attenuators, and divider circuits. Figure 5 shows two 14-bit multiplying CMOS D/A converters.

Another important D/A converter design takes advantage of the best features of both the weighted current source technique and the R-2R ladder technique. This circuit, shown in Figure 6, uses equal values switched current sources to drive the junctions of the R-2R ladder network. The advantage of the equal current source currents is obvious since all emitter resistors are identical and switching speeds are also identical. This technique is used in many ultra-high speed D/A converters.

Glitches can be virtually eliminated by the circuit shown in Figure 7(b). The digital input to a D/A converter is controlled by a set of switches which connect the D/A output to a specially designed sample-hold circuit. When the digital input is updated by the strobe, the sample-hold is switched into the hold mode. After the D/A has changed to its new output value, all switches have settled out, the sample-hold is then switched back into the tracking mode. When this happens, the output changes smoothly from its previous value to the new value with no glitches present.
Analog-To-Digital Converters

Counter Type A/D Converter

Analog-to-digital converters, also called ADCs or encoders, employ a variety of different circuit techniques to implement the conversion function. As with D/A converters, however, relatively few of these circuits are widely used today. Of the various techniques available, the choice depends on the resolution and speed required.

One of the simplest A/D converters is the counter, or servo, type. This circuit employs a digital counter to control the input of a D/A converter. Clock pulses are applied to the counter and the output of the D/A is stepped up one LSB at a time. A comparator compares the D/A output with the analog input and stops the clock pulses when they are equal. The counter output is then the converted digital word.

The operation of this converter is analogous to weighing an unknown on a laboratory balance scale using standard weights in a binary sequence such as 1, 1/2, 1/4, 1/8, . . . , 1/2^k kilograms. The correct procedure is to begin with the largest standard weight and proceed in order down to the smallest one. The largest weight is placed on the balance pan; if it does not tip, the weight is removed and the next one added. If the balance does tip, the weight is removed and the next one added. The same procedure is used for the next largest weight and so on down to the smallest. After the nth standard weight has been tried and a decision made, the weighing is finished. The total of the standard weights remaining on the balance is the closest possible approximation to the unknown.

Successive-Approximation A/D Converters

In the successive-approximation A/D converter, illustrated in Figure 2, a successive-approximation register (SAR) controls the D/A converter by implementing the weighing logic just described. The SAR first turns on the MSB of the DAC and the comparator tests this output against the analog input. A decision is made by the comparator to leave the bit on or turn it off after which bit 2 is turned on and a second comparison made. After n comparisons the digital output of the SAR indicates all those bits which remain on and produces the desired digital code. The clock circuit controls the timing of the SAR. Figure 3 shows the D/A converter output during a typical conversion.

The conversion efficiency of this technique means that high resolution conversions can be made in very short times. For example, it is possible to perform a 10 bit conversion in 1 μsec, or less on a 12 bit conversion in 2 μsec, or less. Of course the speed of the internal circuitry, in particular the D/A and comparator, are critical for high speed performance.

The Parallel (Flash) A/D Converter

For ultra-fast conversions, required in video signal processing and radar applications, where up to 8 bits resolution is required, a different technique is employed. This is known as the parallel (also flash, or simultaneous) method and is illustrated in Figure 4.

This method employs 2^n-1 analog comparators to directly implement the quantizer transfer function of an A/D converter. The comparator trip-points are spaced 1 LSB apart by the series resistor chain and voltage reference. For a given analog input voltage all comparators biased below the voltage turn on and all those biased above it remain off. Since all comparators change state simultaneously, the quantization process is a one-step operation.

A second step is required, however, since the logic output of the comparators is not in binary form. Therefore an ultra-fast decoder circuit is employed to make the logic conversion to binary. The parallel technique reaches the ultimate in high speed because only two sequential operations are required to make the conversion.

The limitation of the method, however, is in the large number of comparators required even for moderate resolutions. A 4-bit converter, for example, requires only 15 comparators, but an 8-bit converter needs 255. For this reason it is common practice to implement an 8-bit A/D with two 4-bit stages as shown in Figure 5.

Figure 1. Tracking Type A/D Converter

While this converter is simple, it is also relatively slow. An improvement on this technique is shown in Figure 3 and is known as a tracking A/D converter, a device commonly used in control systems. Here an up-down counter controls the D/A, and the clock pulses are directed to the pertinent counter input depending on whether the D/A output must increase or decrease to reach the analog input voltage.

The obvious advantage of the tracking A/D converter is that it can continuously follow the input signal and give updated digital output data if the signal does not change too rapidly. Also, for small input changes, the conversion can be quite fast. The converter can be operated in either the track or hold modes by a digital input control.

Successive-Approximation A/D Converters

By far, the most popular A/D conversion technique in general use for moderate to high speed applications is the successive-approximation type A/D. This method falls into a class of techniques known as feedback type A/D converters, to which the counter type also belongs. In both cases a D/A converter is in the feedback loop of a digital control circuit which changes its output until it equals the analog input. In the case of the successive-approximation converter, the DAC is controlled in an optimum manner to complete a conversion in just n steps, where n is the resolution of the converter in bits.
The result of the first 4-bit conversion is converted back to analog by means of an ultra-fast 4-bit D/A and then subtracted from the analog input. The resulting residue is then converted by the second 4-bit A/D, and the two sets of data are accumulated in the 8-bit output register.

Another class of A/D converters known as integrating type operates by an indirect conversion method. The unknown input voltage is converted into a time period which is then measured by a clock and counter. A number of variations exist on the basic principle such as single-slope, dual-slope, and triple-slope methods. In addition there is another technique—which exactly balances the input current—hence the name charge balancing. This balance has the following relationship:

\[ f = \frac{V_{IN}}{R_2} \quad \frac{V_{REF}}{R_1} \]

where \( f \) is the pulse width and \( f \) the frequency. A higher input voltage therefore causes the integrator to ramp up and down faster, producing higher frequency output pulses. The timer circuit sets a fixed time period for counting. Like the dual-slope converter, the circuit also integrates input noise, and if the timer is synchronized with the noise frequency, infinite rejection results. Figure 10 shows the noise rejection characteristic of all integrating type A/D converters with rejection plotted against the ratio of integration period to noise period.
Glossary of analog-to-digital conversion Terms

ABSOLUTE ACCURACY: The worst-case input to output error of a data converter referred to the NBS standard volt.

ACCURACY: The conformance of a measured value to a true value; the maximum error of a device such as a data converter from the true value. See relative accuracy and absolute accuracy.

ADC: Abbreviation for analog-to-digital converter. See A/D converter.

A/D CONVERTER: Analog-to-digital converter. A circuit which converts an analog (continuous) voltage or current into an output digital code.

BCD: See Binary Coded Decimal.

BINARY CODE: See Natural Binary Code.

BINARY CODED DECIMAL (BCD): A binary code used to represent decimal numbers in which each digit from 0 to 9 is represented by four bits weighted 8-4-2-1. Only 10 of the 16 possible states are used.

BIPOLAR MODE: For a data converter, when the analog signal range includes both positive and negative values.

BIPOLAR OFFSET: The analog displacement of one half of full scale range in a data converter operated in the bipolar mode. The offset is generally derived from the converter reference circuit.

CHARGE BALANCING A/D CONVERTER: An analog-to-digital conversion technique which employs an operational integrator circuit within a pulse generating feedback loop. Current pulses from the feedback loop are precisely balanced against the analog input by the integrator, and the resulting pulses are counted for a fixed period of time to produce an output digital word. This technique is also called quantized-feedback.

CLOCK: A circuit in an A/D converter that generates timing pulses which synchronize the operation of the converter.

CLOCK RATE: The frequency of the timing pulses of the clock circuit in an A/D converter.

COMPANDING CONVERTER: An A/D or D/A converter which employs a logarithmic transfer function to expand or compress the analog signal range. These converters have large effective dynamic ranges and are commonly used in digitised voice communication systems.

COMPLEMENTARY BINARY CODE: A binary code which is the logical complement of straight binary: All 1's become 0's and vice versa.

CONVERSION TIME: The time required for an A/D converter to complete a single conversion to specified resolution and linearity for a full scale analog input change.

CONVERSION RATE: The number of repetitive A/D or D/A conversions per second for a full scale change to specified resolution and linearity.

COUNTER TYPE A/D CONVERTER: A feedback method of A/D conversion whereby a digital counter drives a D/A converter which generates an output ramp which is compared with the analog input. When the two are equal, a comparator stops the counter and output data is ready. Also called a servo type A/D converter.

DATA CONVERTER: An A/D or D/A Converter.

DATA WORD: A digital code-word that represents data to be processed.

DIFFERENTIAL LINEARITY ERROR: The maximum deviation of any quantizer (LSB change) in the transfer function of a data converter from its ideal size of FSR/2^n.

DIFFERENTIAL LINEARITY TEMPO: The change in differential linearity error with temperature for a data converter; expressed in ppm/°C of FSR (Full Scale Range).

DIGITALIZER: A device which converts analog into digital data; an A/D converter.

DUAL SLOPE A/D CONVERTER: An indirect method of A/D conversion whereby an analog voltage is converted into a time period by an integrator and reference and then measured by a clock and counter. The method is relatively slow but capable of high accuracy.

DYNAMIC ACCURACY: The total error of a data converter or conversion system when operated at its maximum specified conversion rate or throughput rate.

DYNAMIC RANGE: The ratio of full scale range (FSR) of a data converter to the smallest difference it can resolve. In terms of converter resolution: Dynamic Range (DB) = 20 lb en|log(2^n) = 6.02n where n is the resolution in bits.

ENCODER: A communications term for an A/D converter.


FEEDBACK TYPE A/D CONVERTER: A class of analog-to-digital converters in which a D/A converter is enclosed in the feedback loop of a digital control circuit which changes the D/A output until it equals the analog input.

FSR: Full Scale Range.


FULL SCALE RANGE (FSR): The difference between maximum and minimum analog values for an A/D converter input or D/A converter output.

GAIN ERROR: The difference in slope between the actual and ideal transfer functions for a data converter or other circuit. It is expressed as a percent of analog magnitude.

GAIN TEMPO: The change in gain (or scale factor) with temperature for a data converter or other circuit, generally expressed in ppm/°C.

HYSTERESIS ERROR: The small variation in analog transition points of an A/D converter whereby the transition level depends on the direction from which it is approached. In most A/D converters this hysteresis is very small and is caused by the analog comparator.

INDIRECT TYPE A/D CONVERTER: A class of analog-to-digital converters which converts the unknown input voltage into a time period and then measures this period.

INTEGRAL LINEARITY ERROR: The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

INTEGRATING A/D CONVERTER: One of several types of A/D conversion techniques whereby the analog input is integrated with time. This includes dual slope, triple slope, and charge balancing type A/D converters.

LEAST SIGNIFICANT BIT (LSB): The rightmost bit in a data converter code. The analog size of the LSB can be found from the converter resolution: LSB Size = FSR/2^n where FSR is full scale range and n is the resolution in bits.

LINEARITY ERROR: See Integral Linearity Error and Differential Linearity Error.

LONG TERM STABILITY: The variation in data converter accuracy due to time changes alone. It is commonly specified in percent per 1000 hours or per year.

LOW-LEVEL MULTIPLEXING: An analog multiplexing system in which a low amplitude signal is first multiplexed and then amplified. LSB: Least Significant Bit.

LSB SIZE: See Quantum.

MAJOR CARRY: See Major Transition.

MINIMUM OFFSET: A specified or measured offset value of an analog bipolar D/A converter or other circuit.

OFFS: Data co

PARA

PRECI

PRECISION DIFFICULTY: Precision and term used to describe the conversion errors due to noise and other factors.

PROGRAMMABLE A/D CONVERTER: The combination of an analog-to-digital converter and a processor to produce a computer interface to the data converter.

POWER CHANGE: Power supplied to an A/D or D/A converter.

PRECISION DIFFICULTY: Precision and term used to describe the conversion errors due to noise and other factors.

PROCESSOR: A computer interface to the data converter.

REPEATED LINEARITY: The difference between conversion points of the same input when the converter is repeatedly converted.

ZERO: Offs

ZOE
MAJOR TRANSITION: In a data converter, the change from a code of 1000...000 to 0111...1111 or vice-versa. This transition is the most difficult one to make from a linear standpoint since the MSB weight is ideally precisely one LSB larger than the sum of all other bit weights.

MISSING CODE: In an A/D converter, the characteristic whereby not all output codes are present in the transfer function of the converter. This is caused by a nonmonotonic D/A converter inside the A/D.

MONOTONICITY: For a D/A converter, the characteristic of the transfer function whereby an increasing input code produces a continuously increasing analog output. Nonmonotonicity may occur if the converter differential linearity error exceeds ± LSB.

MOST SIGNIFICANT BIT (MSB): The leftmost bit in a data converter code. It has the largest weight, equal to one half of full scale range.

MSB: Most Significant Bit.

NATURAL BINARY CODE: A positive weighted code in which a number is represented by

\[ N = a_02^0 + a_12^1 + a_22^2 + a_32^3 + \ldots + a_n2^n \]

where each coefficient "a" has a value of zero or one. Data converters use this code in its fractional form where

\[ N = a_12^{-1} + a_22^{-2} + a_32^{-3} + \ldots + a_n2^{-n} \]

and N has a fractional value between zero and one.

NOISE REJECTION: The amount of suppression of normal mode analog input noise of an A/D converter or other circuit, generally expressed in dB. Good noise rejection is a characteristic of integrating type A/D converters.

NORMAL-MODE REJECTION: The attenuation of a spectrum of frequencies appearing directly across two electrical terminals. In A/D converters, normal-mode rejection is determined by an input filter or by integration of the input signal.

OFFSET BINARY CODE: Natural binary code in which the code word 1000...000 is displaced by two positions, divided into a coarse (fast slope) measurement and a fine (slow slope) measurement.

QUANTIZATION NOISE: See Quantization Error.

QUANTIZATION UNCERTAINTY: See Quantization Error.

QUANTIZER: A circuit which transforms a continuous analog signal into a set of discrete output states. Its transfer function is the familiar staircase function.

QUANTIZING ERROR: The inherent uncertainty in digitizing an analog value due to the finite resolution of the conversion process. The quantized value is uncertain by up to ±Q where Q is the quantum size. This error can be reduced only by increasing the resolution of the converter. Also called quantization uncertainty or quantization noise.

QUANTUM: The analog difference between two adjacent codes for an A/D or D/A converter. Also called LSB size.

R-2R LADDER NETWORK: An array of matched resistors with series values of R and shunt values of 2R in a standard ladder circuit configuration.

RATIOMETRIC A/D CONVERTER: An analog-to-digital converter which uses a variable reference to measure the ratio of the input voltage to the reference.

RELATIVE ACCURACY: The worst case input to output error of a data converter, as a percent of full scale, referred to the converter reference. The error consists of offset, gain, and linearity components.

RESOLUTION: The smallest change that can be distinguished by an A/D converter or produced by a D/A converter. Resolution may be stated in percent of full scale, but is commonly expressed as the number of bits n where the converter has 2^n possible states.

SAR: Successive approximation register. A digital control circuit used to control the operation of a successive approximation A/D converter.

SCALE FACTOR ERROR: See Gain Error.

SPAN: For an A/D or D/A converter, the full scale range or difference between maximum and minimum analog values.

START-CONVERT: The input pulse to an A/D converter which initiates conversion.

STATIC ACCURACY: The total error of a data converter or conversion system under DC input conditions.

STATUS OUTPUT: The logic output of an A/D converter which indicates whether the device is in the process of making a conversion or the conversion has been completed and output data is ready. Also called busy output or end of conversion output.

STRAIGHT BINARY CODE: See Natural Binary Code.

SUCCESSIVE APPROXIMATION A/D CONVERTER: An A/D converter that compares a set of increasing binary weighted values with the analog input to produce an output digital word in just a few steps, where n is the resolution bits. This process is efficient and is analogous to weighing an unknown quantity on a balance scale using a set of binary standard weights.

TEMPERATURE COEFFICIENT: The change in analog magnitude with temperature, expressed in ppm/°C.

THREE-STATE OUTPUT: A type of A/D converter output used to connect to a data bus. The three output states are logic 1, logic 0, and off. An enable control turns the output on or off.

TRACKING A/D CONVERTER: A counter-type analog-to-digital converter which can continuously follow the analog input at a specified maximum rate and continuously update its digital output as the input signal changes. The circuit uses a D/A converter driven by an up-down counter.

TRANSFER FUNCTION: The input to output characteristic of a device such as a data converter expressed either mathematically or graphically.

TRIPLE-SLOPE A/D CONVERTER: A variation on a dual slope type A/D converter in which the time constant is divided into N sections, each of 1/N th of full scale, and the ramp generator is turned on and off once per cycle. The circuit uses a ramp-to-zero comparator to measure the time that the ramp is in the non-zero region.

OFFSET DRIFT: The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C or ppm/°F.

OFFSET ERROR: The error at analog zero for a data converter operating in the bipolar mode.

ONE'S COMPLEMENT CODE: A bipolar binary code in which positive and negative codes of the same magnitude sum to all ones.

PARALLEL TYPE A/D CONVERTER: An ultra high-speed A/D conversion method which employs one comparator to directly implement a quantizer where it is in the resolution bits. The quantizer is followed by a decoder circuit which converts the comparator outputs into binary code.

PROPAGATION TYPE A/D CONVERTER: A type of A/D conversion method which employs one comparator to directly implement a quantizer where it is in the resolution bits. The quantizer is followed by a decoder circuit which converts the comparator outputs into binary code.

POWER SUPPLY SENSITIVITY: The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in mV/° or mV/% supply change.

PRECISION: The degree of repeatability, or reproducibility of a series of successive measurements. Precision is affected by the noise, hysteresis, time and temperature stability of a data converter or other device.